Isabel Leonard
Medical and Technical Translation
5 Hearn Street, Watertown, MA 02472-1502, USA
Phone 617-661-3273 Fax 617-441-0036
e-mail: isabelleonard@comcast.net

File 7867

VERIFICATION OF TRANSLATION

I hereby declare and state that I am knowledgeable of each of the German and English languages and that I made and reviewed the attached translation of the patent application entitled: "Storage Device for a Multibus Architecture" from the German language into the English language, and that I believe my attached translation to be accurate, true, and correct to the best of my knowledge and ability.

Date: January 16, 2004

Isabel A. Leonard
Translator

WESTPHAL, MUSSGNUG & PARTNER

European Patent Attorneys

MICRONAS GmbH

Hans-Bunte-Strasse 19

79108 Freiburg

- Patent Application -

Storage Device for a Multibus Architecture

Storage Device for a Multibus Architecture

The invention relates to a storage device for a multibus architecture having the features listed in the preamble of Claim 1, a storage system having a plurality of storage devices, and a method for controlling such a storage device.

In order to achieve a high throughput of data in signal processors, these often include multiple connected read/write buses through which one data memory may be accessed simultaneously. Control of memory addresses is implemented here through read/write buses by alternately transmitting address data and information data, or by transmitting addresses through a separate address bus.

In the case of these systems involving one or multiple data memories in multiple buses, that is, a multibus architecture, the actual connection is achieved in a manner which is disadvantageous. Currently, two approaches are commonly utilized to achieve efficient memory access to store data in the memory, or to read data from the memory. Either a multi-port memory is used which has multiple memory connections to access different buses, or the various buses are connected only to mutually independent memory blocks.

The first approach has the disadvantage that a multi-port memory is more complex and expensive to implement than a single-port memory. The second approach has the disadvantage that the separation of memory blocks negatively affects program flexibility and execution speed. For example, the memory partitioning must be defined within the program code – a capability which is often not provided in high-level languages such as C.

The goal of the invention is therefore to propose a storage device for a multibus architecture which enables more efficient memory access. An additional goal is to propose a storage system having a plurality of such storage devices, as well as a method for operating such storage devices.

This goal is achieved by a storage device for a multibus architecture having the features of Claim 1, a storage system having a plurality of storage devices with the features of Claim 9, and a method for controlling such a storage device having the features of Claim 12.

The starting point of the invention is a storage device for a multibus architecture which comprises at least one memory to store data, information, and/or addresses and a memory connection with a port to connect the memory to a first bus of a multibus architecture, wherein the memory connection, the port, and the first bus have data lines to transmit data and, as required, address lines to transmit addresses, and/or control information to control the memory and, as required, other devices connected to each the specific bus.

A switching device serves to selectively connect the memory connection to the first bus or an additional bus to enable a memory access to transmit data, addresses, and/or control information from or to these buses. A storage system, specifically a storage system within a processor or directly connected to a processor, advantageously has a plurality of such storage devices which are selectively connected, according to the method, to one each of the different buses.

Advantageous embodiments are the subject of the dependent claims.

The storage device advantageously has a memory-specific logic device and an interrupt line to transmit an interrupt signal to the processor, which processor controls the entire system, whereby transmission of the interrupt signal triggers an interruption of the operation of the processor for one clock cycle whenever a memory access by the memory to the memory or memories of two different buses within two successive clock cycles is to be effected.

The memory advantageously has an address analyzer to analyze the addresses on the buses and/or the address lines assigned to the memory for memory accesses, and for the purpose of switching the switching device to one of the corresponding buses.

The analyzer serves to analyze address segments and to switch and assign memory access for address segments smaller than the word width of a bus or of address lines transmitting the addresses, such that the memory may be smaller than the actual required memory space. Additional data for storage are stored in a different memory.

An adjustable separator device, specifically a programmably adjustable separator device for storing the memory address or access address for the memory for analysis by the analyzer allows the memory to assign any addresses in order, for example, to be able to overlay external memories.

The analyzer advantageously has a common access control device to switch the switching device, and one comparator each per bus to compare the address with the memory address of the memory, thereby allowing the component-related expense to be reduced.

The analyzer advantageously has includes a modifier designed to process different data and/or access types which are applied – through data lines, subaddress lines, and/or access signal lines selected by the switching device – to a data memory segment of the memory in order to transmit the states on the bus lines.

A logic device to output a block loss signal through a loss line to the processor serves to issue a signal in response to a deviation from announced and executed data transfers during the memory access.

A preferred storage system has a plurality of such memories which are connected to a multibus architecture having a plurality of buses. It is possible here to have all of the memories or only some of the memories connectable only to some of the buses.

Specifically, during switching between read access and write access for one of the memories, different memories are controlled alternately by clock cycle in a common process.

The use of such memories is advantageous particularly in the form of memories for a processor.

An interrupt signal to suspend the processor clock of a higher-level processor or to select a different memory is advantageously generated and issued whenever a

memory access by the memory to two different buses, or by two different buses to the memory, is to be effected within two successive clock cycles in order to prevent loss of data.

Having the processor use the logic device to generate a command such as a clock control signal to interrupt the processor clock or such as a memory select signal to select a different storage device, and send this signal to the processor prevents loss of data or drop-out periods during switching operations between read states and write states.

For memory accesses, address lines on the buses assigned to the memory, or address lines for determining the switching position of the switching device, are analyzed.

It is also possible here to search address segments smaller than the word width of the address as the assigned memory address during the analysis and to use them as the switching criterion – this being advantageous for the distribution of data between multiple memories of this type.

To this end, a method may be used in which the highest-value bit of the address to determine the access address is compared with an adjustable register, specifically a programmable register, and the memory access is enabled only in the case of a match.

This procedure may be employed for example to implement an overlay procedure in which another memory, specifically a slower and larger memory is overlaid.

In order to control a switching device, selected data lines, subaddress lines, and/or access signal lines of a selected bus are used to generate switching signals or commands in the event data or information transmitted over the selected bus does not match, in terms of the amount of data, the amount of memory space available per memory access operation.

The following discussion explains embodiments of the invention in more detail based on the drawings

Figure 1 is a schematic view of a storage device including a memory which may be connected to a multibus architecture using a switching device; and

Figure 2 shows a preferred storage device including a detailed illustration of individual preferred components of a logic device to control the switching device.

Figure 1 shows how one embodiment of a storage device is connected to a multibus architecture, here including three buses P, D0, D1. The devices and functions shown and described here are only examples used to explain the basic principle of a memory M which may be selectively connected through a switching device SW to one of multiple buses P, D0, D1 of the multibus architecture. Any additional components that might be required to operate such a storage device, such as address buses and other control buses, may be added in accordance with the commonly available technical knowledge.

A memory M of this type is in the form of and configured as memory M in a multibus architecture of a processor PU according to the preferred embodiment. Processor PU

appropriately has a storage system including a plurality of such memories M, of which one bus each is able to be controlled simultaneously for a memory access. Memory access here means both the writing to memory M of data, specifically, information data, and the reading of this data from a memory area of memory M through one of buses P, D0, D1. The illustrated buses P, D0, D1 lead directly to processor PU, although the relevant required control devices, interface components, and the like are not shown since these may be implemented in the conventional manner. The same applies to control lines BML, STL which transmit, for example, a block loss signal bm, or an interrupt signal st, or other commands.

The actual memory or memory area M of the storage device has a memory connection B in the form of a memory port of the conventional type. The memory connection is connected to switching device SW through data lines DL or through the data lines DL of a data bus. Switching device SW selectively switches data lines DL through corresponding lines PL, D0L, D1L and external ports BP, B0, B1 to one of buses P, D0 or D1.

Logic device L serves to switch switching device SW, which logic device is connected preferably to additional devices such as a memory separator register (memory tag register) MTR and at least one comparator CU. The block loss line BML here starts, for example, from comparator CU and leads to processor PU, while interrupt signal line STL leads from the actual logic device L to processor PU.

In a preferred embodiment, a conventional common data memory is subdivided into multiple blocks functioning as the storage system of processor PU, which blocks, like memory M shown, have only a single internal access connection B. Multiple read/write buses P, D0, D1 are connected to each of these memories M through switching device SW. The logic device integrated within the block acts as an access control device and controls the memory access of the different buses to the block and to memory M located in the block, or of memory M to one of buses P, D0, D1. It is not absolutely necessary, of course, that each of memories M be connectable to all of buses P, D0, D1.

Whenever two of buses P, D0, D1 are to simultaneously access the same memory M, logic device L sends the interrupt signal st through interrupt signal line STL to processor PU or to a clock control device of processor PU so as to suspend the clock for the processor for one clock cycle, thereby allowing switching device SW to switch successive accesses to the two requesting buses and the corresponding states to be transmitted on the bus lines. Alternatively, appropriate programming and/or an appropriate wiring layout of processor PU is able to handle the suspension of the clock.

Specifically, write access is possible in smaller units than the word width of the buses without losing a clock cycle, that is, for example, byte-by-byte accessing for a 32-bit bus. The actual read-modify-write operation here requires the usual two clock cycles. In order to prevent the loss of a clock cycle, either buffering is implemented by logic device L on the incoming side of memory M and by any other devices connected to this device, or an appropriate access control signal st is exchanged with the processor PU in order that

this memory M not be acted upon during the next clock cycle so that processor PU does not need to be suspended, but instead accesses a different memory M during this next clock cycle.

The memory-block-specific logic device L is advantageously expandable by using a comparator CU which compares the highest-value bit of the address with an adjustable register – specifically, a register adjustable by programming – and only operates in the case of a match, with the result that the individual memories M of a plurality of such memories M are able to be arranged in any fashion within a linear address space. For example, a memory of a slow external memory module may be overlaid by a memory access to memory M, then copied back upon termination of a corresponding dedicated program segment. This method, in fact well known as the overlay procedure, enables fast access to the data despite the fact that the internal memory M of the processor may be smaller than the memory required for the application. A relatively larger required memory area is thus appropriately managed by splitting among multiple smaller memories M.

Memory M in Figure 1 has only one data line or databus DL. In principle, it is possible to transmit address data and information data in temporal sequence over a single bus, where the address data indicate to which, or from which, memories M or addresses within memory M the information data are to be transmitted as the actual data d. Alternatively, it is possible to employ a separate address bus through which exclusively address data are transmitted, with the result that only actual useful data, and possibly additional address or control information, are transmitted through databus DL.

Figure 2 illustrates a detailed embodiment, in which again a memory M having preferably a plurality of addressable memory locations is connectable through switching device SW to one of multiple buses P, D0, D1, R of a multibus architecture.

In the example shown, memory connection B is subdivided into an address memory connection and a data memory connection. The addresses for addressing internal memory locations of memory M, which are transmitted through a separate address bus or, as described above, through one of buses P, D0, D1, R, are applied to the address memory connection. In the embodiment shown, in each case the address information is supplied from the actively switched bus P.

It is possible specifically here also to have addresses supplied only through a bus P in the form of a programming bus such that switching device SW implements switching to programming bus P routinely or upon completion of a memory access. To implement a data access, the switch-over to the required additional bus D0, D1, R is effected as required.

Starting from buses P, D0, D1, R, which may, for example, be 32-bit buses, a 32-bit line leads to a data input switch of switching device SW. Depending on the switching position of switching device SW, a 32-bit data line or a 32-bit databus DL is thus routed from the selected bus P, D0, D1, R through switching device SW to the data memory connection of data connection B in order to write or read the relevant data or line states to or from the memory area of memory M addressed at this moment.

Data line DL which leads from each bus P, D0, D1, R to the corresponding switching connection of switching device SW has a splitter SP at the input of logic device L composed of a plurality of individual components, which splitter is, for example, in the form of a tap, wherein the individual data lines of databus DL are tapped and routed as address lines AL to a divider DIV. In this example, divider DIV separates out ten address lines AL and routes these to an appropriately connected address line input of switching device SW. Depending on the switching position, the address signal of the selected bus P, D0, D1, R is thus applied to the address memory input of address connection B of memory M.

In addition, two address lines SAL are separated out from divider DIV to transmit subaddresses, then routed to an appropriately connected input of switching device SW which passes on the subaddress of the selected bus P, D0, D1, R to a modifier MOD.

The splitter SP also splits the data lines – for example, four of lines ACL with information about the access type – from the actual data lines 32 and routes these to an appropriately connected input of switching device SW. This device also applies the signals or states of address type lines ACL to modifier MOD depending on the switching position of selected bus P, D0, D1, R.

Modifier MOD is also interconnected between the switched data line DL and data memory connection B. Modifier MOD serves to modify the received data d from selected bus P, D0, D1, R and determines, in terms of the access type, specifically

a write access or read access, whether what is found on data line DL is a complete word, shortened word (short), or only one byte from an original data word which is to be transmitted during the memory access, or if it is a label or signal that has been extended in some way.

In addition, modifier MOD, among other functions, passes on a read-modifier-write signal to an access control device ARB forming an additional component of logic device L. In connection with processor PU, access control device ARB controls access to memory M. Access control device ARB additionally controls the operation of switching device SW.

Memory logic L, as the analyzer or part of the analyzer, also advantageously has a memory separator register or memory tag register MTR which is programmable, for example through bus R, with the access address of memory M. Memory tag register MTR advantageously also has an overflow line AGL to provide memory overflow protection.

Address lines AL, here 20 of the address lines, branch off from divider DIV, each of which are routed to a comparator CU. Comparator CU compares the thus received address data with the address data stored in memory tag register MTR and provides the comparison result to access control device ARB for further processing.